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10/044,217	11/19/2001	Robert M. Zeidman	6257-16302	9153

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EXAMINER	
LUU, CUONG V	

ART UNIT	PAPER NUMBER
2128	

NOTIFICATION DATE	DELIVERY MODE
02/05/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/044,217	ZEIDMAN, ROBERT M.	
	Examiner	Art Unit	
	Cuong V. Luu	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *64-70 and 72-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *64-70 and 72-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 64-70 and 72-85 are pending. Claims 81-85 have been added. Claims 1-63 and 71 have been canceled. Claims 64-70 and 72-85 have been examined. Claims 64-70 and 72-85 have been rejected.

Response to Arguments

1. The 35 U.S.C. 112, first paragraph rejection of claim 71 has been withdrawn in light of its cancellation.

2. Applicant's arguments filed 12/30/2009 have been fully considered but they are not persuasive. The Applicant's arguments are mainly about Evans' not teaching different transmission rates of a computer's receiving data packets and sending data packets. In col. 10 lines 5-24, Evans teaches the time for transmitting data to the computer 118 from computer 114 is slower than that of circuit of a hardware modeled. The emulator is a hardware modeled and operates at a frequency relatively close to actual anticipated one as acknowledged in this paragraph. Therefore, Evans acknowledges that the frequency of communication between the emulator and the computer 114 is faster than that of communication between the simulation computer 118 and the computer 114. It would have been obvious for one of ordinary skill in the art to use the same system connection to implement data transfer to have the second speed slower than the first speed. Claims 64-69 and 72-85, therefore, are rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 64-69 and 72-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of the Applicant's Admitted Prior Art, hereinafter the AAPA, page 1 line 9 through page 2 line 14 in view of Evans et al. (U.S. Pat. 6,279,146 B1).

1. As per claim 64, the AAPA teaches system, comprising:

a computer configured to couple to an emulator, wherein the emulator is configured to emulate a design of an integrated circuit having a network interface (p. 2 line 4-7. The AAPA teaches an emulator connected to a network, transmitting and receiving signals from the network. The teaching of receiving signals from the network implies that a computer is coupled to said emulator. In addition, the emulator can communicate with the network, so it implies that the emulator is configured to emulate a design of an integrated circuit having a network interface);

wherein the computer is configured to receive one or more data packets at a first transmission rate p. 2 line 4-7. The AAPA teaches an emulator connected to a network, transmitting and receiving signals from the network. The teaching of receiving signals from the network implies that a computer is coupled to said emulator and receiving data packets at a first speed);

but does not teach:

wherein the computer is configured to:

buffer the data packets; and

send data contained in the buffered data packets to the emulator at a second transmission rate, wherein the second transmission rate is slower than the first transmission rate.

Evans teaches:

wherein a computer is configured to receive data packets at a first transmission rate (Fig. 2. Computer 118 is connected to computer 114 for communication, so it reads onto this limitation);

wherein the computer is configured to:

send data to the emulator at a second speed (col. 9 line 17-28).

However, Evans does not teach the second transmission rate is slower than the first transmission rate but the first speed is slower than the second speed (col. 10 lines 5-24. In these lines Evans teaches the time for transmitting data to the computer 118 from computer 114 is slower than that of circuit of a hardware modeled. The emulator is a hardware modeled and operates at a frequency relatively close to actual anticipated one as acknowledged in this paragraph. Therefore, Evans acknowledges that the frequency of communication between the emulator and the computer 114 is faster than that of communication between the simulation computer 118 and the computer 114). It would have been obvious for one of ordinary skill in the art to use the same system connection to implement data transfer to have the second speed slower than the first speed.

Gagne teaches buffering the data packets (col. 1 lines 60-68 and col. 2 lines 1-2).

It would have been obvious to one of ordinary skill in the art to combine the teachings of the AAPA, Gagne, and Evans. Gagne's and Evans's teachings would have provided buffers dedicated to different destinations (Gagne, col. 1 lines 60-68 and col. 2 lines 1-2) and speed

up the verification time of an emulator having a network interface with easy interconnection (col. 2 lines 37-38 and col. 3 lines 63-67).

2. As per claim 65, the AAPA teaches the emulator is configured to receive and process the sent data according to the design of the integrated circuit (col. 10 lines 5-24.).

3. As per claim 66, Gagne teaches the computer is configured to, for each incoming data packet:

examine that data packet (col. 1 line 60 through col. 2 line 2. In these lines Gagne teaches receiving data and put them in proper buffers for different destination. This teaching implies that data packets are examined);

determine if that data packet is addressed to the emulator (col. 1 line 60 through col. 2 line 2. In these lines Gagne teaches receiving data and put them in proper buffers for different destination. This teaching reads onto this limitation); and

if that data packet is addressed to the emulator, buffer that data packet and send data contained in the buffered packet to the emulator (col. 1 line 60 through col. 2 line 2. In these lines Gagne teaches receiving data and put them in proper buffers for different destination. This teaching reads onto this limitation).

4. As per claim 67, the AAPA teaches the emulator is incapable of receiving and processing data sent at the first transmission rate (p. 1 lines 16-20).

5. As per claim 68, the AAPA teaches wherein the emulator is implemented, at least in part, using field programmable gate arrays (p. 1 lines 15-18); and

wherein the field programmable gate arrays are operable to be programmed with a hardware model corresponding to the design of the integrated circuit (p. 1 lines 15-18).

6. As per claim 69, Evans teaches wherein the second computer is further configured to repackage data from the buffered data packets (col. 9 lines 17-28);

wherein the repackaged data is the data the second computer is configured to send to the emulator at the second speed (this limitation has already been discussed in claim 64. It is, therefore, rejected for the same reasons).

7. As per claim 72, Evans teaches another computer is configured to generate the one or more packets to be sent to the second computer (col. 9 lines 17-28); and

Gagne teaches the generated packets are variable in size (col. 1 lines 60-68 and col. 2 lines 1-2).

8. As per claim 73, the AAPA teaches a method, comprising:

a first computer receiving a plurality of data packets at a first transmission rate, wherein the data packets are received over a network connection (p. 2 line 4-7. The AAPA teaches an emulator connected to a network, transmitting and receiving signals from the network. The teaching of receiving signals from the network implies that a computer corresponding to a first computer in this limitation is coupled to a network);

the first computer sending data contained in the buffered packets to an emulator, wherein the emulator is configured to emulate a design of an integrated circuit used as a component of a network communication device (p. 2 line 4-7. The AAPA teaches an emulator connected to a network, transmitting and receiving signals from the network. The

teaching of receiving signals from the network implies that a computer is coupled to said emulator. In addition, the emulator can communicate with the network, so it implies that the emulator is configured to emulate a design of an integrated circuit having a network interface);

However, the AAPA does not teach:

buffering one or more of the plurality of data packets; and

the first computer sending data to the emulator at a second transmission rate, which is slower than the first transmission rate.

Gagne teaches buffering one or more of the plurality of data packets (col. 1 lines 60-68 and col. 2 lines 1-2); and

Evans suggests a computer sending data to an emulator at a transmission rate, which is faster than the transmission rate of said computer receiving data packets (see discussion in claim 64).

It would have been obvious to one of ordinary skill in the art to combine the teachings of the AAPA, Gagne, and Evans. Gagne's and Evans's teachings would have provided buffers dedicated to different destinations (Gagne, col. 1 lines 60-68 and col. 2 lines 1-2) and sped up the verification time of an emulator having a network interface with easy interconnection (col. 2 lines 37-38 and col. 3 lines 63-67).

9. As per claim 74, the AAPA teaches the data sent to the second computer is usable to debug the design of the integrated circuit (p. 1 lines 10-12); and

wherein the network connection is an Ethernet connection (p. 1 lines 18-20).

10. As per claim 75, these limitations have already been discussed in claim 69. They are, therefore, rejected for the same reasons.

11. As per claim 76, this limitation has been discussed in claim 65. It is, therefore, rejected for the same reasons.

12. As per claim 77, Evans teaches the emulator sending data corresponding to the received and processed data to a second computer (col. 9 lines 17-28).

13. As per claim 78, the AAPA teaches the emulator is configured to emulate a network interface card of the second computer (p. 1 lines 23-26. In these lines the AAPA teaches the emulator process data and transmit data. This teaching is interpreted as transmitting data to a second computer after the emulator having a network interface receiving data, so it should read onto this limitation); and

wherein the data is sent to the second computer via a bus coupled to the emulator (data is inherently sent via a bus).

14. As per claim 79, these limitations have already been discussed in claim 66. They are, therefore, rejected for the same reasons.

15. As per claim 80, these limitations have already been discussed in claim 68. They are, therefore, rejected for the same reasons.

16. As per claim 81, these limitations have already been discussed in claim 64. They are, therefore, rejected for the same reasons.

17. As per claim 82, these limitations have already been discussed in claim 66. They are, therefore, rejected for the same reasons.

18. As per claim 83, these limitations have already been discussed in claim 68. They are, therefore, rejected for the same reasons.

19. As per claim 84, these limitations have already been discussed in claim 69. They are, therefore, rejected for the same reasons.

20. As per claim 85, these limitations have already been discussed in claim 67. They are, therefore, rejected for the same reasons.

Claims 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over in view of the Applicant's Admitted Prior Art, hereinafter the AAPA, page 1 line 9 through page 2 line 14 in view of Evans et al. (U.S. Pat. 6,279,146 B1) and Gagne et al. (5,303,347) as applied to claim 65 above, and further in view of Watanabe et al (U.S. Pat. 5761486).

21. As per claim 70, the AAPA, Evans, and Gagne do not teach the second computer is further configured to log data corresponding to received data and/or sent data in a log file.

However, Watanabe teaches keeping a record of communicated data from source to destination (col. 6 lines 18-23)

It would have been obvious to one of ordinary skill in the art to combine the teachings of the AAPA, Evans, and Gagne, and Watanabe. Watanabe's teachings would have provided designers information of the emulation in order to analyze and evaluate the emulation (col. 3 lines 43-51).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah, can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. An inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Cuong V Luu/

Examiner, Art Unit 2128

/Hugh Jones/

Primary Examiner, Art Unit 2128